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10/528,255	03/17/2005	Martin J. Edwards	GB03 0024 US	4146

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EXAMINER	
CHOWDHURY, AFROZA Y	
ART UNIT	**PAPER NUMBER**
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/528,255	EDWARDS, MARTIN J.	
	Examiner	Art Unit	
	Afroza Y. Chowdhury	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-8* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/17/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 should be designated by a legend such as –Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: In page 8, line 9, "**a column drive 40**" should be "**a column drive 42**".

Appropriate correction is required.

Claim Objections

3. Claim 1 is objected to because of the following informalities: "**sub-pixels (P1 – P4)**" should be changed to "**sub-pixels**".

Claim 5 is objected to because of the following informalities: "**any one of claim 1**" should be changed to "**claim 1**".

Claim 6 is objected to because of the following informalities: "**any one of claim 1**" should be changed to "**claim 1**".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicant Admitted Prior Art** (herein AAPA) in view of **Ozawa et al**. (US Pub. 2002/0018056) and in further view of **Kimura** (US Patent 2002/0044109).

As to claim 1, AAPA teaches an active matrix display device comprising an array of pixels a set of row conductors (fig. 1(14)) through which rows of pixels are selected (page 1, lines 11-15, page 2, lines 27-29),

a set of column conductor (fig. 1(15)) through which data signals are supplied to selected pixels (page 1, lines 11-15, page 2, lines 24-27),

each pixel comprising a plurality of sub pixels (fig. 1(P1-P4)), and

which sub pixels (fig. 1(P1-P4)) are each associated with a respective switching transistor (fig. 1(T1-T4)) for controlling the supply of a data signal to the sub pixel (page 2, lines 24-27, page 1, lines 11-15).

AAPA does not teach an active matrix display device wherein a plurality of sub pixels of a pixel are coupled to a column conductor associated with the pixel via a common switching transistor through which data signals are supplied to the sub pixels, and the device is operable in a first mode in which the plurality of sub-pixels of a pixel are addressed simultaneously with a data signal and in a second mode in which the sub pixels of a pixel are addressed individually with respective data signals.

Ozawa et al. discloses a display device wherein the device is operable in a first mode in which the sub pixels of a pixel are addressed individually with respective data signals ([0095] – [0097]) and

in a second mode in which the plurality of sub-pixels of a pixel are addressed simultaneously with a data signal ([0102]).

Therefore, it is obvious to one skill in the art at the time of the invention was made to include the technique of addressing a plurality of sub-pixels with data signals of Ozawa et al. into AAPA's driving method of an active matrix display device in order to make a display device with increased gradation capability ([0012], in Ozawa et al.).

Ozawa et al. does not teach a display device wherein a plurality of sub pixels of a pixel are coupled to a column conductor associated with the pixel via a common switching transistor through which data signals are supplied to the sub pixels.

Kimura discloses a display device wherein a plurality of sub pixels of a pixel are coupled to a column conductor associated with the pixel via a common switching transistor (fig. 1(ST11)) through which data signals are supplied to the sub pixels (fig.1, [0045] – [0046])).

Therefore, it is obvious to one skill in the art at the time of the invention was made to incorporate Kimura's idea of using a common switching transistor through which data signals are supplied to a plurality of sub pixels into the active matrix display device of AAPA (as modified by Ozawa et al.) to make smaller and lower power-consuming display device ([0021], in Kimura).

As to claim 2, AAPA (as modified by Ozawa et al. and Kimura) teaches a display device wherein the device comprises drive means for providing data signals to the column conductors and switching signals to the row conductors (page 1, lines 11-15 in AAPA), and

wherein the drive means is operable in the second mode to switch the switching transistors associated with the sub pixels of the pixel selectively in sequence such that data signals on the associated column conductor are supplied to respective sub pixels ([0095] – [0097], in Ozawa et al.), and

wherein the drive means is operable in the first mode to switch the switching transistors associated with the sub pixels of a pixel at the same time so as to supply a data signal on the associated column conductor to each sub pixel ([0102], in Ozawa et al.).

As to claim 3, AAPA (as modified by Ozawa et al.) does not explicitly teach a display device where the sub pixels of a pixel are connected in serial manner with the input terminal of the switching transistor associated with the first sub pixel of the series being connected to the associated column address conductor and with the input terminal of the switching transistor associated with each of the other sub pixels in the series being connected to the output terminal of the switching transistor associated with the preceding sub pixel in the series.

However, it is obvious to combine Kimura's idea of using a common switching transistor through which data signals are supplied to a plurality of sub pixels into the active matrix display device of AAPA (as modified by Ozawa et al.) to make a display device where the sub pixels of a pixel are connected in serial manner with the input terminal of the switching transistor associated with the first sub pixel of the series being connected to the associated column address conductor and with the input terminal of the switching transistor associated with each of the other sub pixels in the series being connected to the output terminal of the switching transistor associated with the preceding sub pixel in the series.

As to claim 4, AAPA (as modified by Ozawa et al.) does not specifically teach a display device wherein the sub pixels of a pixel are connected in parallel manner with the input terminal of the switching transistor associated with one sub pixel being connected to the associated column address conductor and with the input terminals of

the switching transistors associated with the other sub pixels being connected to the output terminal of the switching transistor associated with the one pixel.

However, it is obvious to combine Kimura's idea of using a common switching transistor through which data signals are supplied to a plurality of sub pixels into the active matrix display device of AAPA (as modified by Ozawa et al.) to make a display device where the sub pixels of a pixel are connected in serial manner with the input terminal of the switching transistor associated with the first sub pixel of the series being connected to the associated column address conductor and with the input terminal of the switching transistor associated with each of the other sub pixels in the series being connected to the output terminal of the switching transistor associated with the preceding sub pixel in the series.

As to claim 5, AAPA (as modified by Ozawa et al. and Kimura) teaches a display device wherein the control electrodes of the switching transistors associated with the sub pixels of a pixel are connected to respective different row conductors (figs. 2, in Ozawa et al.).

As to claim 7, AAPA (as modified by Ozawa et al. and Kimura) teaches a display device wherein the sub pixels comprise liquid crystal picture elements connected to the outputs of their associated switching transistor (figs. 2, 4, in Ozawa et al.).

As to claim 8, AAPA (as modified by Ozawa et al. and Kimura) teaches a display device where at least two sub pixels of a pixel are of different areas (fig. 3, [0066], in Ozawa et al.).

Allowable Subject Matter

6. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

None of the prior art references, above or in combination, teach or fairly suggest the limitation of:

"**a display device wherein each pixel (P) comprises first and second sub pixels, wherein the control electrodes of the switching transistors associated with the first and second sub pixels of a pixel are connected to first and second row conductors respectively,**

wherein for each pixel, the input of the switching transistor associated with the first sub pixel is connected to the associated column conductor and the input of the switching transistor associated with the second sub pixel is connected to the output of the switching transistor associated with the first sub pixel,

wherein the first row conductor connected to one pixel is connected also to the control electrode of the switching transistor associated with the second sub pixel of another pixel connected to the associated column conductor, and

wherein the second row conductor connected to the one pixel is connected also to the control electrode of the switching transistor associated with the first sub pixel of a further pixel connected to the associated column address conductor" in claim 6.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Afroza Y. Chowdhury whose telephone number is 571-270-1543. The examiner can normally be reached on 7:30-5:00 EST, 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shawlwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC
1/26/2008

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